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Grain Size and Interface Dependence of Bias Stress Stability of n-Type Organic Field Effect Transistors

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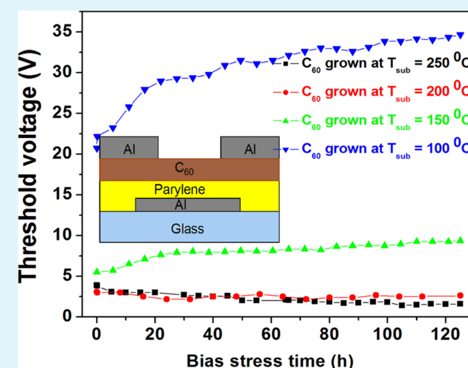
ABSTRACT: The effect of grain size and interface dependence of bias stress stability of C_{60}-based n-type organic field effect transistors (OFETs) has been studied. It has been realized that, with increasing grain size of C_{60}, the bias stress induced threshold voltage shift can be controlled and this effect is mainly attributed to the mechanism of charge trapping at grain boundaries. It is further studied that the growth of C_{60} on the surface of parylene at elevated substrate temperature leads to the creation of radicals at the interface between the active layer and the gate dielectric. These radicals help to improve the bias stress stability of C_{60}-based n-type OFETs. For achieving the bias stress stability, we have presented a procedure of creation of radicals at the interface between C_{60} and parylene in single gate OFETs instead of dual gate OFETs.



KEYWORDS: *C_{60}, bias stress, n-type OFETs stability, threshold voltage shift, charge trapping in semiconductor and dielectric interface, grain boundaries, parylene*

1. INTRODUCTION

Potentials for the uses of organic semiconductors in large area devices, such as light emitting diodes,[1] drivers for flexible display,[2] organic solar cells,[3] photodetectors,[4] and identification tags made them interesting for researchers to improve their performance.[5] The main factors which can aggravate the performance of the organic field effect transistors (OFETs) are the low charge carrier field effect mobility,[6] environmental stability,[7,8] and bias stress reliability.[9,10] The major hindrances in overcoming these inhibiting factors are the poor knowledge of charge transport in organic semiconductors and the nature of degradation mechanisms under bias stress and in ambient environment. A strong improvement in the knowledge of these obstacles is a primary key in the optimization of the performance of OFETs. The operation of OFETs relys on the charge injection at source drain contacts,[11] the degree of crystallinity of the active layer,[12−14] and the interface between the dielectric and the organic semiconductor layer.[15] According to the aspect of electronic circuit design, besides the high charge carrier mobility, reliability of OFETs is an important issue. Already some efforts have been made to perform reliable studies of p-type and n-type OFETs.[16−19] The bias stress stability of p-type OFETs was measured,[20] and it was inferred that the barrier height for charge trapping can be controlled by using self-aasembled monolayers (SAMs) on the surface of the gate dielectric. It was reported that increasing the barrier height for charge trapping can decrease the bias stress effects. It was observed that the charge trapping also has some dependence on the surface morphology of the active layer. The bias stress effect in pentacene OFETs was studied with different dielectrics.[21] It was reported that the fabrication of devices stable against bias stress is possible by using appropriate gate dielectric layers. The trapped charges were visualized in real time using scanning Kelvin probe microscopy (SKPM)[22] and it was reported that the charges are trapped at the surface of the gate dielectric, instead of the semiconducting layer.

In a recent article, the bias stress effects on C_{60} based n-type OFETs have been discussed comprehensively. The experimental results reveal that, during the bias stress, the charges can be trapped in the organic semiconductor as well as in the gate insulator layers. The bias stress induced charge trapping is 10 times faster in the active layers as compared to the gate insulator layer. The charge trapping in the active layer can be controlled by depositing the organic semiconductors at elevated substrate temperatures, while the selection of an appropriate gate insulator can also decrease the bias stress effects up to 55%.[23] From the literature, it can be easily deduced that during bias stress the charges can be trapped in the active layer, in the gate dielectric, or at the interface between gate dielectric and organic semiconductor and these trapped charges induce a threshold voltage shift.[24,25]

In our recent article,[26] it was reported that dual gate OFETs are more stable against bias stress as compared to single gate OFETs. However, fabrication of dual gate OFETs is

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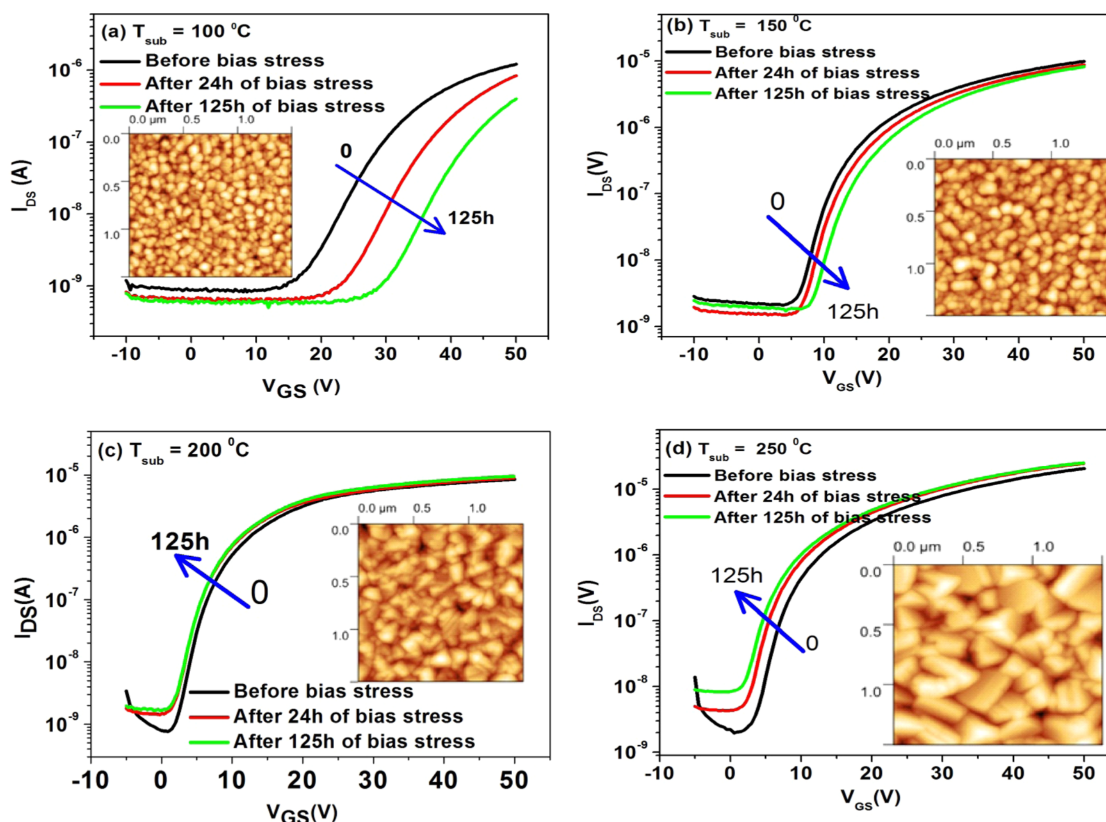

Figure 1. Transfer characteristics measured before bias stress, after 24 h of bias stress, and after 125 h of bias stress time with C_{60} grown at (a) T_{sub} = 100 °C, (b) T_{sub} = 150 °C, (c) T_{sub} = 200 °C, and (d) T_{sub} = 250 °C.

complicated as compared with single gate OFTEs and it also requires additional experimental efforts. The main concealed feature of dual gate OFETs which is responsible for the bias stress stability is the modified interface due to the formation of radicals.[27] In the present work, we have demonstrated that these radicals which are responsible for the stability of OFETs against bias stress can be created in single gate OFETs. Therefore, the bias stress stability of OFETs in more simple geometrical structures can be achieved.

2. EXPERIMENTAL DETAILS

The experimental procedure for the fabrication of OFETs was almost the same as that used in our previous studies.[23,28] The OFETs were fabricated by using glass substrates. Before the fabrication of OFETs, the glass substrates were cleaned using acetone and deionized water in an ultrasonic bath and dried in a nitrogen flow. The gate electrode having a thickness of 100 nm and a width 0.5 mm was evaporated by using a shadow mask in a vacuum of 10^{-6} mbar. The parylene layer as gate dielectric was deposited on the surface of the gate electrode using a homemade parylene evaporation system which works with a three-zone process. In the first zone the parylene was evaporated at 100 °C. In the second zone the parylene vapor has to pass through a high temperature zone (750 °C), where pyrolysis leads to a cleavage of the dimers. In the last zone the monomers are deposited on the surface of the gate electrode at room temperature. For the fabrication of OFETs, 1 μm thick parylene layers were deposited as the gate dielectric. A 200 nm thick layer of C_{60} (MER Corp.) was deposited by hot wall epitaxy (HWE) in a vacuum of 10^{-6} mbar with different substrate temperatures T_{sub} = 100, 150, 200, and 250 °C, a source temperature of T_s = 360 °C, and a wall temperature of T_{wall} = 400 °C. For top contact electrodes, 70 nm thick Al was evaporated under high vacuum (10^{-6} mbar), using a shadow mask. The channel length L and width W in the OFETs were 70 μm and 1.5 mm, respectively. After the evaporation of C_{60} in the HWE reactor, the device was transported to the glovebox in ambient conditions. All the measurements were performed inside the glovebox in a nitrogen controlled environment. The gate voltage was applied by a Keithley 6487 Pico-Ampere meter, and the same was used for measuring the leakage current and the transfer characteristics. The source−drain voltage was applied by a Keithley 2400 voltage source unit, and the same was used for monitoring the output characteristics. For applying the bias stress, the source−drain voltage was varied from 0 to 50 V and the gate−source voltage was varied from −10 to +50 V. All the measurements were automatically controlled by a computer switch, and all experimental data points were registered by a Metlab program.

3. RESULTS AND DISCUSSION

For the fabrication of OFETs, the growth of C_{60} active layers was done by the HWE system. The HWE system has three ovens, named the source oven, wall oven, and substrate oven. The source oven was used to evaporate the organic material (C_{60}) and the wall oven was used to avoid unnecessary depositions on the walls of the tube between source and substrate, while the substrate oven was used to control the surface mobility of the impinging molecules and in that way the morphology of the deposited material. Therefore, in an HWE system, it was possible to vary the grain size and crystallinity of the film by varying the substrate temperature. C_{60} was grown at four different substrate temperatures (T_{sub}) of 100, 150, 200, and 250 °C. The bottom gate top contact OFETs were fabricated with four different morphologies of the active layer while keeping the dielectric layer the same (parylene with capacitance density 1.77 × 10^{-9} F/cm^2). The four OFETs, fabricated with C_{60} grown at four different substrate temperatures, were installed in the measurement setup for applying bias stress. The continuous bias stress was applied for 125 h to

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each device, and the transfer characteristics were registered. The transfer characteristics measured before bias stress, after 24 h of bias stress, and after 125 h of bias stress are presented in the Figure 1. The atomic force microscopic (AFM) images of C_{60} grown at different substrate temperatures are also presented as insets in the corresponding device characteristics. It is quite evident from the AFM images that the grain size in the C_{60} layer increases as the substrate temperature increases. The structural analysis of the C_{60} layers deposited at different substrate temperatures depicts that the crystallinity can be improved by depositing C_{60} layers at elevated substrate temperatures.[29] Figure 1 clearly illustrates that the devices fabricated with C_{60} layers grown at elevated substrate temperatures show better performance as compared to the devices fabricated with C_{60} layers grown at lower substrate temperatures. The bias stress stability of OFETs is a major issue.[10] The transfer characteristic measured after 24 h of bias stress is shifted toward the transfer characteristic measured after 125 h of bias stress time. This means that, in the initial hours of continuous bias stress, it shifts rapidly and then slowly reaches a saturated value. The shift in the transfer characteristic can be attributed to the bias stress induced threshold voltage shift. The threshold voltage was measured for the whole period of investigation and is presented in Figure 2 along with a

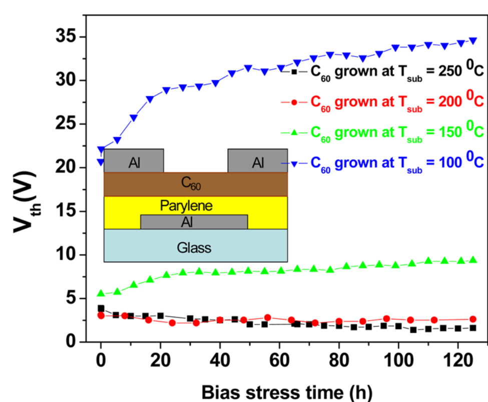

Figure 2. Threshold voltage shift with bias stress time.

geometrical sketch of the OFET as an inset. During the entire period of investigations, the threshold voltage was stable in the OFETs fabricated with C_{60} grown at substrate temperatures of 200 and 250 °C, while the OFETs fabricated with C_{60} grown at substrate temperatures of 100 and 150 °C, show a shift in the threshold voltage. It is worth noting that the direction of threshold voltage shift in the OFETs fabricated with C_{60} layers grown at T_{sub} = 200 and 250 °C is opposite that for the devices fabricated at lower T_{sub} = 100 and 150 °C.

In a recent article,[23] it has been reported that increasing the grain size or decreasing the grain boundaries within the OFET channel improves the stability of the threshold voltage against bias stress. The threshold voltage shift measured in the devices fabricated at T_{sub} = 100 and 150 °C is in good agreement with earlier reports, but the threshold voltage shifts observed in the devices fabricated with active layer grown at T_{sub} = 200 and 250 °C are not in line with the previous reports.[23] It is evident from Figure 2 that the threshold voltage shift in the OFETs fabricated with C_{60} grown at higher substrate temperature (T_{sub} = 250 °C) has larger values compared to the OFETs fabricated at lower substrate temperature (T_{sub} = 200 °C), which is contrary to our earlier results.[23] The electron trapping is believed to be the main reason for the shift in the threshold voltage in n-type OFETs.[30] A similar type of threshold voltage shift to more positive V_{GS} has been already reported for another n-type organic semiconductor, namely, perylene diimide derivative PTCDI-$C_{13}H_{27}$.[31] In the present work, the parylene was used as a gate dielectric. The reactivity of C_{60} and parylene can be found in the literature.[32] Furthermore, it has been already reported that the evaporation of parylene on C_{60} layers can create radicals and the formation of a clean interface (free of radicals) between the active layer and the gate dielectric is only possible by depositing C_{60} layers on the surface of parylene but not vice versa.[27] Therefore, the creation of such radicals is reported in top-gate bottom-contact OFETs but not in bottom-gate top-contact OFETs. It has been discussed in detail that the presence of these radicals at the interface between C_{60} and parylene can cause the bias stress induced threshold voltage shift to more negative V_{GS}.[26]

In the fabrication process of bottom-gate OFETs, the parylene monomers evaporated at 100 °C through the high temperature zone (750 °C) to the deposition chamber held at room temperature and polymerize at the surface of the glass substrate. After the pyrolysis, the conformal thin parylene films are thermally stable up to 200 °C.[33] Therefore, if we treat the parylene thin films around 200 °C or higher, then there is a finite probability that cross-linked dimers can reopen their side chains or become thermally activated. Consequently, while deposition of C_{60} on the surface of parylene at a substrate temperature around 200 °C or higher, there is a finite probability that the thermally activated parylene monomers may react with C_{60} instead of polymerize with each other. The reactivity of C_{60} with parylene can create radicals,[27] and these radicals can cause the bias stress induced threshold voltage shift toward the more negative V_{GS}.[26] The threshold voltage shift toward the more negative V_{GS} in the OFETs fabricated with active layers grown at substrate temperatures of 200 and 250 °C confirms our assertion that the radicals are formed at the interface. Therefore, the threshold voltage shift toward the more negative V_{GS} can be attributed to the creation of radicals at the C_{60} and parylene interface and our present study is in good agreement with the earlier reports.[26,27]

Besides the bidirectional threshold voltage shift in our device, it was also observed that the threshold voltage shift in the OFET fabricated at T_{sub} = 150 °C is less compared to that in the OFET fabricated at T_{sub} = 100 °C. The parylene thin film is thermally stable up to 200 °C; therefore, this reduction cannot be associated with the creation of radicals at the interface between the C_{60} and parylene. However, this reduction in the value of bias stress induced threshold voltage shift is related to the grain boundaries.[23] From the AFM images, it is also obvious that the grain size of C_{60} increases with the increase of substrate temperature during the growth of active layers. The OFETs fabricated with C_{60} grown at higher substrate temperatures (200, 250 °C) have a larger grain size of C_{60} as compared to the OFETs fabricated with C_{60} grown at lower substrate temperatures (100, 150 °C). The decrease in the bias stress induced threshold voltage shift with an increase in the grain size of C_{60} is quite evident from Figure 1a,b. The experimental results reveal that increasing the grain size or decreasing the grain boundaries within the OFET channel improves the bias stress stability of OFETs. Therefore, it is very hard to exclude the correlation of grain size with the threshold voltage shift in the OFETs fabricated with C_{60} grown at higher substrate temperatures (200, 250 °C), having the larger grain size as

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compared to the C_{60} grown at substrate temperatures (100, 150 °C). In other words, the bias stress stability, observed in the OFETs fabricated with active layer grown at T_{sub} = 200 °C, can be conceived as the combined effect of grain boundaries[23] as well as the creation of radicals at the interface between the active layer and gate dielectric.[26,27]

The creation of radials in the single gate devices provides us several benefits: (1) For achieving bias stress stability, the number of experimental steps are decreased and stability of on/off ratio is improved (see Figure 1c) as compared to dual gate OFETs.[26] (2) By combining the effect of grain boundaries and creation of radicals, it is possible to decrease the temperature of the growth of the active layer from 250 to 200 °C for threshold voltage stability,[23] which will provide us an opportunity to fabricate OFETs on plastic/flexible substrates.[2] (3) Threshold voltage stability in C_{60}-based OFETs can be achieved with low price dielectric (parylene) layers instead of high price dielectric (benzocyclobutene (BCB), etc.).[23] All these benefits are helpful in decreasing the cost of fabrication of C_{60}-based OFETs.

4. CONCLUSION

In summary, the effect of grain size and interface dependence of bias stress stability of C_{60}-based n-type OFETs is reported. It is shown that, by increasing the grain size of C_{60}, the bias stress induced threshold voltage shift can be controlled and this effect is mainly attributed to the mechanism of charge trapping related to the grain boundaries. It is also found that the growth of C_{60} on the surface of parylene at higher substrate temperatures (200, 250 °C) leads toward the creation of radicals at the interface between the active layer and the gate dielectric. These radicals can help in improving the bias stress stability of C_{60}-based n-type OFETs. For the bias stress stability, we have presented a procedure of creation of radicals at the interface between the C_{60} and parylene in single gate OFETs instead of dual gate OFETs.[26]

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Notes

The authors declare no competing financial interest.

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